IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Chen et al.

Examiner: WEISS, H.

Serial No.:

10/697,589

Art Unit: 2814

Filed:

October 30, 2003

Confirmation No.: 8317

For:

Po no Terbo

METHOD FOR MAKING NANOSCALE WIRES AND GAPS FOR SWITCHES AND

TRANSISTORS

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

AMENDMENTS AND REMARKS

Dear Sir:

In response to the Office Action mailed April 13, 2005, and per the Request for Continued Examination filed herewith, please consider the following remarks and enter the following amendments.

Amendments to the specification are presented on page 2 of this response. Amendments to the claims are presented beginning on page 3 of this response. Remarks begin on page 7 of this response.

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